



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application:

Application No.:

Filed:

Title:

Commissioner for patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE OF ENTIRE INTEREST
(REVOCATION OF PRIOR POWERS)

As assignee of record of each of the patent applications listed in the table of attachment A,

REVOCATION OF PRIOR POWERS OF ATTORNEY

all powers of attorney previously given in each of the listed patent applications are hereby revoked, and

NEW POWER OF ATTORNEY

the following attorneys/agents are hereby appointed to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: I hereby appoint all attorneys of Thomas, Kayden, Horstemeyer & Risley, LLP, who are listed under the USPTO Customer Number shown below as the attorneys to prosecute this application and to transact all business in the United States Patent and Trademark Office connected therewith, recognizing that the specific attorneys listed under that Customer Number may be changed from time to time at the sole discretion of Thomas, Kayden, Horstemeyer & Risley, LLP, and request that all correspondence about the application be addressed to the address filed under the same USPTO Customer Number.

24504

Patent Trademark Office

Please direct all future correspondence and telephone calls to:

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Date: 9/9/04



Chien-Wei (Chris) Chou
Director - Intellectual Property Division



ASSIGNEE CERTIFICATION

The certification under 37 C.F.R. §3.73(b) establishing the right of assignee to take action is attached hereto along with documentation evidencing same. Further, in my official position with Taiwan Semiconductor Manufacturing Company, Ltd., I am authorized to sign documents and otherwise act on its behalf in connection with the management and handling of patent applications and other intellectual property matters.

Date: 9/9/04



Chien-Wei (Chris) Chou
Director - Intellectual Property Division



Attachment A

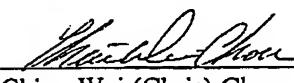
No.	Serial No	Application Title	Filing Date	Assignment (Reel/Frame)
1.	10/310,486	A Method of Process Simplification and Eliminating Topography Concerns for the Creation of Advanced IT-RAM Devices	12/05/02	013556/0586
2.	10/861,149	A Novel Device Structure Having Enhanced Surface Adhesion and Failure Mode Analysis	06/04/04	
3.	10/861,148	Self-Aligned Electrode to Eliminate Native Oxide Effect for Metal Insulator Semiconductor (MIS) Capacitor	06/04/04	
4.	10/861,132	Method and System for Merging Wafer Test Results	06/04/04	
5.	10/017,955	Localized Slots for Stress Relieve in Copper	12/14/01	012386/0945
6.	10/845,887	Localized Slots for Stress Relieve in Copper	05/14/04	Recorded 012386/0945 at the parent application USP 10/017,955
7.	10/602,337	Redundancy Structure in Self-Aligned Contact Process	06/24/03	Recorded _____ / _____ at the parent application USP 6,597,055
8.	10/655,689	SBGA Design for Low-K Integrated Circuits (IC)	09/05/03	014471/0048
9.	10/462,314	Shallow Trench Isolation Structure with Low Sidewall Capacitance for High Speed Integrated Circuits	06/13/03	014194/0150
10.	10/655,662	Method to Make Minimal Spacing Between Floating Gates in Split Gate Flash	09/05/03	014470/0854
11.	10/042,074	Grid Metal Design for Large Density CMOS Image Sensor	01/08/02	012494/0258

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 Chien-Wei (Chris) Chou
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12.	10/325,951	Method for Forming High Purity Silicon Oxide Field Oxide Isolation Region	06/04/99	010021/0093
13.	10/462,267	Gate Stack for High Performance Sub-Micron CMOS Devices	06/16/03	Recorded 012017/0126 at the parent application USP 6,596,599
14.	10/323,983	A Structure for Split Flash Memory Cells Containing a Programming Injector and a Method for Fabricating the Structure	12/19/02	013618/0294
15.	10/189,910	Stripe Board Dummy Metal for Reducing Coupling Capacitance	07/05/02	013086/0834
16.	10/686,794	Flash EEPROM with Function Bit by Bit Erasing	10/16/03	Recorded 012482/0478 at the parent application USP 6,638,821
17.	10/315,645	Method for Forming a Planarized Bond Pad Structure	12/10/02	013576/0082
18.	10/178,384	Structure and Fabricating Method to Make a Cell with Multi-Self-Alignment in Split Gate Flash	06/24/02	013058/0398
19.	10/821,270	Whole Chip ESD Protection	04/08/04	Recorded 013155/0802 at the parent application USP 6,730,968
20.	10/268,585	New Structures of Vertical Resistors and FETs as Controlled by Electrical Field Penetration and a Band-Gap Voltage Reference Using Vertical FETs Operating in Accumulation Through the Field Penetration Effect	10/10/02	013385/0110

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